DECLARATION

I, Minoru UCHIDA, a national of Japan, c/o Musashi Works of Renesas Technology Corp. of 20-1, Josuihoncho 5-chome, Kodaira-shi, Tokyo, Japan, do hereby solemnly and sincerely declare:

1) THAT I am well acquainted with the Japanese language and English language, and
2) THAT the attached is a full, true and faithful translation into the English language made by me of Japanese Patent Application No. 1995-126405 filed on May 25, 1995.

The undersigned declares further that all statements made herein of his own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 19 day of August, 2009.

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[Title of the Invention] Semiconductor Device and Method for Manufacturing the same

[Claims]

1. A semiconductor device comprising a base substrate, a semiconductor pellet mounted over a pellet mounting area of a main surface of the base substrate, external terminals arranged over a main surface of the semiconductor pellet, and first electrode pads arranged over a back surface of the base substrate and coupled electrically to the external terminals,

wherein the base substrate is a rigid substrate, the first electrode pads of the base substrate are coupled electrically to second electrode pads arranged over the back surface of the base substrate, the semiconductor pellet is mounted over the pellet mounting area of the main surface of the base substrate in a state in which the main surface of the semiconductor pellet faces down, and the external terminals of the semiconductor pellet and the second electrode pads of the base substrate are coupled together electrically using bonding wires through a slit formed in the base substrate.

2. A semiconductor device according to claim 1, wherein the slit is formed in a layout direction of the external terminals arranged plurally over the main surface of the semiconductor pellet and is arranged over the external terminals of the

semiconductor pellet.

3. A semiconductor device according to claim 1 or claim 2, wherein the second electrode pads of the base substrate are arranged respectively in both side areas of the back surface of the base substrate partitioned by the slit.

4. A semiconductor device according to claim 3, wherein electric power is applied to the second electrode pads arranged in one area of the back surface of the base substrate partitioned by the slit, while a signal is applied to each of the second electrode pads arranged in the other area of the back surface of the base substrate partitioned by the slit.

5. A semiconductor device according to any of claims 1 to 4, wherein the back surface of the semiconductor pellet is exposed from a sealing body which covers a peripheral area of the main surface of the base substrate from above.

6. A semiconductor device according to any of claims 1 to 5, wherein the bonding wires are sealed with a resinous sealing body.

7. A semiconductor device according to any of claims 1 to 6, wherein bump electrodes are coupled electrically and mechanically onto surfaces of the first electrode pads of the base substrate.

8. A method for manufacturing a semiconductor device comprising a base substrate, a semiconductor pellet mounted

over a pellet mounting area of a main surface of the base substrate, external terminals arranged over a main surface of the semiconductor pellet, and first electrode pads arranged over a back surface of the base substrate and coupled electrically to the external terminals, the method comprising the steps of mounting a semiconductor pellet over a pellet mounting area of a main surface of a base substrate comprised of a rigid substrate in a state in which a main surface of the semiconductor pellet faces down, and coupling external terminals of the semiconductor pellet and second electrode pads electrically to each other using bonding wires through a slit formed in the base substrate, wherein the second electrode pads are coupled electrically to first electrode pads of the base substrate and arranged over a back surface of the base substrate.

9. A method for manufacturing a semiconductor device according to claim 8, further comprising, after the electrical coupling step using the bonding wires, the step of forming, by a transfer molding method, a resinous sealing body covering a peripheral area of the main surface of the base substrate from above and sealing the bonding wires.

[Detailed Description of the Invention]

[0001]

[Industrial Application Field]

The present invention relates to a semiconductor device and a manufacturing technique for the semiconductor device. Particularly, the present invention is concerned with a technique applicable effectively to both a semiconductor device and a manufacturing technique for the semiconductor device, the semiconductor device comprising a base substrate, a semiconductor pellet mounted on a pellet mounting area of a main surface of a base substrate, external terminals arranged on a main surface of the semiconductor pellet, and first electrode pads arranged on a back surface of the base substrate and connected electrically to the external terminals.

[0002]

[Prior Art]

As a semiconductor device affording a high packaging density, a semiconductor device of a BGA (Ball Grid Array) structure is disclosed, for example, in Nikkei Electronics published by Nikkei MacGraw-Hill, Inc. [February 28, 1994, pp. 111-117]. In the semiconductor device adopting the BGA structure, as shown in Fig. 16 (a sectional view of a principal portion), a semiconductor pellet 2 is mounted on a pellet mounting area of a main surface of a base substrate 1 and plural

bump electrodes 4 are arranged lattice-like on a back surface side opposite to the main surface of the base substrate 1.

[0003]

For example, the base substrate 1 is comprised of a printed wiring substrate of a two-layer wiring structure. Plural electrode pads 1A are arranged in a peripheral area (around the pellet mounting area) of the main surface of the base substrate 1. Moreover, plural electrode pads 1B are arranged on the back surface opposite to the main surface of the base substrate 1. The second electrode pads 1A are connected electrically to through-hole wiring lines 1C via wiring lines $1A_1$ arranged on the main surface of the base substrate 1. The first electrode pads 1B are connected electrically to the through-hole wiring lines 1C via wiring lines $1B_1$ arranged on the back surface of the base substrate 1.

[0004]

The semiconductor pellet 2 is mainly comprised of a semiconductor substrate 2B which is formed of a single crystal silicon for example. A logic circuit system, a memory circuit system, or a mixed circuit system thereof, is mounted on a main surface (an elements-forming surface) of the semiconductor substrate 2B. Plural external terminals (bonding pads) 2A are also arranged on the main surface of the semiconductor substrate 2B. The external terminals 2A are formed in the top wiring layer

out of wiring layers formed on the main surface of the semiconductor substrate 2B.

[0005]

The external terminals 2A of the semiconductor pellet 2 are connected electrically via bonding wires 6 to the second electrode pads 1A arranged on the main surface of the base substrate 1. That is, the external terminals 2A of the semiconductor pellet 2 are connected electrically to the first electrode pads 1B via bonding wires 3, second electrode pads 1A, wiring lines $1A_1$, through-hole wiring lines 1C and wiring lines $1B_1$.

[0006]

The semiconductor pellet 2 and the bonding wires 6 are sealed with a resinous sealing body 7 formed on the main surface of the base substrate 1. The resinous sealing body 7 is formed by a transfer molding method.

[0007]

Bump electrodes 4 are connected electrically and mechanically onto surfaces of the first electrode pads 1B of the base substrate 1. For example, the bump electrodes 4 are formed using Pb-Sn alloy.

[0008]

The semiconductor device of the BGA structure thus configured is mounted onto a mounting surface of a mounting

substrate and the bump electrodes 4 of the semiconductor device are connected electrically and mechanically to the electrode pads arranged on the mounting surface of the mounting substrate.

[0009]

As a semiconductor device affording a high packaging density, a semiconductor device having a flexible base substrate is disclosed, for example, in U.S. Patent No. 5148265. According to the structure of this semiconductor device, a semiconductor pellet is mounted onto a pellet mounting area of a main surface of a base substrate comprised of a flexible substrate in such a manner that a main surface of the semiconductor pellet faces down, and external terminals formed on the main surface of the semiconductor pellet and second electrode pads arranged on a back surface of the base substrate are connected together electrically using bonding wires. The second electrode pads of the base substrate are connected electrically through wiring lines arranged on back surfaces thereof to first electrode pads arranged on the back surfaces. Bump electrodes are connected electrically and mechanically to surfaces of the first electrode pads.

[0010]

The semiconductor device thus configured is mounted onto a mounting surface of a mounting substrate and the bump electrodes thereof are connected electrically and mechanically

to electrode pads arranged on the mounting surface of the mounting substrate.

[0011]

[Problems to be Solved by the Invention]

(1) In the semiconductor device of the BGA structure, as shown in Fig. 16, the second electrode pads 1A arranged on the main surface of the base substrate 1 are connected electrically via through-hole wiring lines 1C to the first electrode pads 1B arranged on the back surface of the base substrate 1. Each through-hole wiring line 1C is comprised of a hole region formed within a through hole in the base substrate 1 and land regions (fringe portions) formed on both main surface and back surface of the base substrate 1. An inside diameter of the through hole is set at, for example, 0.3 mm and an outside diameter of each land region of the through-hole wiring line 1C is set at, for example, 0.6 mm. The inside diameter of the through hole and the outside diameter of each land region of the through-hole wiring line 1C are each set larger than the wiring width of each wiring line $1A_1$ which provides an electrical connection between each second electrode pad 1A and the associated through-hole wiring line 1C and the wiring width of each wiring line $1B_1$ which provides an electrical connection between each first electrode pad 1B and the associated through-hole wiring line 1C.

[0012]

On the other hand, the circuit system mounted on the semiconductor pellet 2 tends to become higher in the degree of integration, and with such a higher integration degree of the circuit system, the number of external terminals 2A of the semiconductor pellet 2 and that of the second electrode pads 1A of the base substrate 1 increase. That is, as the integration degree of the circuit system becomes higher, the number of through-hole wiring lines 1C for electrical connection between the second electrode pads 1A and the first electrode pads 1B increases. Consequently, the outline size of the base substrate 1 becomes larger to a degree corresponding to the increase in the number of through-hole wiring lines 1C, thus giving rise to the problem that the size of the semiconductor device becomes larger.

[0013]

(2) In the semiconductor device of the BGA structure, as the number of through-hole wiring lines 1C increases, the through-hole wiring lines 1C are arranged at distant positions from the semiconductor pellet 2 toward the outside. Consequently, the wiring lines $1A_1$ which provide electrical connections between the second electrode pads 1A and the through-hole wiring lines 1C become longer and so does the wiring lines $1B_1$ which provide electrical connections between the first electrode pads 1B and the through-hole wiring lines

1C, thus giving rise to the problem that the inductance increases and the operating speed of the semiconductor device decreases.

[0014]

(3) In the semiconductor device having a flexible base substrate, the flexible substrate is formed, for example, by a polyester film or a polyimide film. The flexible substrate is low in Young's modulus and soft (low in hardness) as compared with a rigid substrate comprising glass fibers impregnated with, for example, epoxy resin or polyimide resin. Therefore, when connecting the external terminals arranged on the main surface of the semiconductor pellet and the second electrode pads arranged on the back surface of the base substrate electrically with each other using bonding wires, a bonding load to be applied to the second electrode pad is absorbed by the base substrate and both bonding load and ultrasonic oscillation are not effectively transmitted to the second electrode pads. As result, there arises the problem that the connection strength between the bonding wires and the second electrode pads decreases, there occurs a defective connection of bonding wires and the electrical reliability of the semiconductor device is deteriorated.

[0015]

(4) In the semiconductor device having a flexible base

substrate, the flexible substrate is larger in thermal expansion coefficient in a planar direction and lower in Young's modulus so is apt to bend (rigidity is low) as compared with the rigid substrate. As a result, when mounting the semiconductor device onto a mounting surface of a mounting substrate, the base substrate undergoes deformation such as warping or twisting with reflow heat in the mounting process, with consequent deterioration in the degree of flatness of the back surface of the base substrate with respect to the mounting surface of the mounting substrate, thus leading to a lowering of the semiconductor device mounting accuracy.

[0016]

It is an object of the present invention to provide a technique capable of attaining the reduction in size of a semiconductor device.

[0017]

It is another object of the present invention to provide a technique capable of attaining a high operating speed of a semiconductor device.

[0018]

It is a further object of the present invention to provide a technique capable of enhancing the electrical reliability of a semiconductor device.

[0019]

It is a still further object of the present invention to provide a technique capable of enhancing a semiconductor device mounting accuracy.

[0020]

It is a still further object of the present invention to provide a semiconductor device manufacturing technique capable of achieving the above-mentioned objects.

[0021]

The above and other objects and novel features of the present invention will become apparent from the following description and the accompanying drawings.

[0022]

[Means for Solving the Problems]

The following is a brief description of typical modes of the present invention as disclosed herein.

[0023]

(1) A semiconductor device comprising a base substrate, a semiconductor pellet mounted over a pellet mounting area of a main surface of the base substrate, external terminals arranged over a main surface of the semiconductor pellet, and first electrode pads arranged over a back surface of the base substrate and coupled electrically to the external terminals, the base substrate being a rigid substrate, the first electrode pads of the base substrate being coupled electrically to second

electrode pads arranged over the back surface of the base substrate, the semiconductor pellet being mounted over the pellet mounting area of the main surface of he base substrate in a state in which the main surface of the semiconductor pellet faces down, the external terminals of the semiconductor pellet and the second electrode pads of the base substrate being coupled together electrically using bonding wires through a slit formed in the base substrate.

[0024]

(2) A method for manufacturing a semiconductor device comprising a base substrate, a semiconductor pellet mounted over a pellet mounting area of a main surface of the base substrate, external terminals arranged over a main surface of the semiconductor pellet, and first electrode pads arranged over a back surface of the base substrate and coupled electrically to the external terminals, the method comprising the steps of mounting a semiconductor pellet over a pellet mounting area of a main surface of a base substrate comprised of a rigid substrate in a state in which a main surface of the semiconductor pellet faces down, and coupling external terminals of the semiconductor pellet and second electrode pads electrically to each other using bonding wires through a slit formed in the base substrate, the second electrode pads being coupled electrically to first electrode pads of the base

substrate and arranged over a back surface of the base substrate.

[0025]

[Operation]

According to the above means (1), since the external terminals of the semiconductor pellet and the first electrode pads of the base substrate can be coupled together electrically through bonding wires and second electrode pads, it is possible to omit through-hole wiring lines for electrical coupling between the second electrode pads and the first electrode pads. As a result, the outline size of the base substrate can be reduced to a degree corresponding to the area (land region area) occupied by the through-hole wiring lines and hence it is possible to attain the reduction in size of the semiconductor device.

[0026]

Moreover, since the first electrode pads can be drawn nearer to the second electrode pads by a distance corresponding to the area occupied by the through-hole wiring lines, it is possible to shorten the wiring lines of the base substrate for electrical coupling between the second electrode pads and the first electrode pads. As a result, it is possible to decrease inductance and hence possible to attain a high operating speed of the semiconductor device.

[0027]

The rigid substrate is higher in Young's modulus and harder than the flexible substrate, so when coupling the external terminals arranged on the main surface of the semiconductor pellet and the second electrode pads arranged on the back surface of the base substrate electrically with each other through bonding wires, a bonding load to be applied to the second electrode pads is not absorbed by the base substrate and both bonding load and ultrasonic oscillation are transmitted effectively to the second electrode pads. As a result, it is possible to enhance the coupling strength between the bonding wires and the second electrode pads and hence possible to prevent the occurrence of a coupling defect of the bonding wires and enhance the electrical reliability of the semiconductor device.

[0028]

The rigid substrate, in comparison with the flexible substrate, is small in thermal expansion coefficient in a planar direction, high in Young's modulus and difficult to bend, so when mounting the semiconductor device onto a mounting surface of a mounting substrate, it is possible to prevent deformation (e.g., warping or twisting) of the base substrate caused by reflow heat generated in the mounting process. As a result, it is possible to ensure the flatness of the back surface of

the base substrate with respect to the mounting surface of the mounting substrate and hence possible to enhance the semiconductor device mounting accuracy.

[0029]

According to the above means (2), since the external terminals of the semiconductor pellet and the first electrode pads of the base substrate are coupled together electrically through bonding wires and second electrode pads, through-hole wiring lines for electrical coupling between the second electrode pads and the first electrode pads are omitted and it is possible to use a base substrate whose outline size is reduced to a degree corresponding to the area occupied by the through-hole wiring lines. As a result, it is possible to manufacture a semiconductor device of a small outline size.

[0030]

Since the external terminals of the semiconductor pellet and the first electrode pads of the base substrate are coupled together electrically through bonding wires and second electrode pads, through-hole wiring lines for electrical coupling between the second electrode pads and the first electrode pads are omitted and it is possible to use a base substrate having wiring lines for electrical coupling between the second electrode pads and the first electrode pads which wiring lines are shorter to a degree corresponding to the area

occupied by the through-hole wiring lines. As a result, it is possible to manufacture a semiconductor device having a high operating speed.

[0031]

The base substrate used is a rigid substrate high in Young's modulus and hard as compared with a flexible substrate, so when coupling the external terminals arranged on the main surface of the semiconductor pellet and the second electrode pads arranged on the back surface of the base substrate electrically with each other using bonding wires, a bonding load to be applied to the second electrode pads is not absorbed by the base substrate and both bonding load and ultrasonic oscillation are transmitted effectively to the second electrode pads. As a result, it is possible to enhance the coupling strength between the bonding wires and the second electrode pads and hence possible to manufacture a semiconductor device high in electrical reliability.

[0032]

The base substrate used is a rigid substrate small in thermal expansion coefficient, high in Young's modulus and difficult to bend as compared with a flexible substrate, so when mounting the semiconductor device onto a mounting surface of a mounting substrate, it is possible to prevent deformation (e.g., warping or twisting) of the base substrate caused by

reflow heat generated in the mounting process. As a result, it is possible to ensure the flatness of the back surface of the base substrate with respect to the mounting surface of the mounting substrate and hence possible to manufacture a semiconductor device high in mounting accuracy.

[0033]

[Embodiments]

The construction of the present invention will be described hereinunder by way of embodiments thereof in which the present invention is applied to semiconductor devices each adopting a BGA structure.

[0034]

In all the drawings for illustrating the embodiments, portions having the same functions are identified by the same reference numerals, and repeated explanations thereof will be omitted.

[0035]

(First Embodiment)

A schematic construction of a semiconductor device adopting a BGA structure according to a first embodiment of the present invention is shown in Fig. 1 (a plan view on a main surface side), Fig. 2 (a sectional view taken on line A-A in Fig. 1), Fig. 3 (an enlarged sectional view of a principal portion in Fig. 2) and Fig. 4 (an enlarged plan view of a

principal portion on a back side with a resinous sealing body on the back side removed).

[0036]

In the semiconductor device of this first embodiment, as shown in Figs. 1, 2, 3 and 4, a semiconductor pellet 2 is mounted on a pellet mounting area of a main surface of a base substrate 1 and plural bump electrodes 4 are arranged lattice-like on a back surface side opposite to the main surface of the base substrate 1.

[0037]

The base substrate 1 is, for example, a printed wiring substrate. The printed wiring substrate is comprised of a rigid substrate and wiring lines formed on a surface of the rigid substrate, the rigid substrate comprising glass fibers impregnated with, for example, epoxy resin, polyimide resin or maleimide resin. That is, the base substrate 1 is comprised of such a rigid substrate. The rigid substrate is high in Young's modulus and hard as compared with a flexible substrate formed, for example, by a polyester film or a polyimide film. Moreover, the rigid substrate, as compared with the flexible substrate, is small in thermal expansion coefficient in a planar direction, high in Young's modulus and difficult to bend. For example, a rigid substrate formed by impregnating glass fibers with epoxy resin or polyimide resin has a Young's modulus of

about 16 - 22 [GPa] and a thermal expansion coefficient of about 10 - 20×10^{-6} [1/°C]. The flexible substrate formed by a polyester film or a polyimide film has a Young's modulus of about 2 - 5 [GPa] and a thermal expansion coefficient of about 20 - 25×10^{-6} [1/°C].

[0038]

Plural second electrode pads 1A and plural first electrode pads 1B are arranged on the back surface of the base substrate 1. The second electrode pads 1A and the first electrode pads 1B are respectively connected with each other electrically through wiring lines $1B_1$ arranged on the back surface of the base substrate 1. The second electrode pads 1A, the first electrode pads 1B and the wiring lines $1B_1$ are each formed by a Cu film for example.

[0039]

The bump electrodes 4 are connected onto surfaces of the first electrode pads 1B electrically and mechanically. For example, the bump electrodes 4 are formed of Pb-Sn alloy.

[0040]

The semiconductor pellet 2 is mounted on the pellet mounting area of the main surface of the base substrate 1 in a state in which a main surface (a lower surface in Figs. 2 and 3) of the semiconductor pellet faces down. That is, the semiconductor pellet 2 is mounted in a face-down manner onto

the pellet mounting area of the main surface of the base substrate 1. An insulating layer 3 is interposed between the main surface of the semiconductor pellet 2 and the pellet mounting area of the main surface of the base substrate. The insulating layer 3 is formed of resin low in elasticity such as, for example, polyimide resin, epoxy resin, or silicon resin.

[0041]

For example, the semiconductor pellet 2 is formed in a rectangular shape in plan. The semiconductor pellet 2 is mainly comprised of a semiconductor substrate 2B which is formed of a single crystal silicon for example. A logic circuit system, a memory circuit system, or a mixed circuit system thereof, is mounted on a main surface (elements-forming surface) of the semiconductor substrate 2B. Moreover, on the main surface of the semiconductor substrate 2B, plural external terminals (bonding pads) 2A are arranged along each side of the rectangular shape. The external terminals 2A are formed in the top wiring layer out of wiring layers formed on the main surface of the semiconductor substrate 2B. That is, along the outer periphery of the main surface of the semiconductor pellet 2 there are arranged plural external terminals 2A for each side.

[0042]

The external terminals 2A on each side of the semiconductor pellet 2 and the associated second electrode pads

1A on the base substrate 1 are connected together electrically with bonding wires 6 through a slit 5 formed in the base substrate 1. For example, the bonding wires 6 are each formed by gold (Au) wire, copper (Cu) wire, aluminum (Al) wire, or a coated wire obtained by coating the surface of a metal wire with an insulating resin. The bonding wires 6 are bonded for example by a thermosonic wire bonding method.

[0043]

The slit 5 is formed in the arranged direction of the external terminals 2A arranged plurally along one side of the main surface of the semiconductor pellet 2. The slit 5 is formed for each side of the semiconductor pellet 2. That is, four slits 5 are formed in the base substrate 1 used in this embodiment. The four slits 5 are formed over the external terminals 2A respectively on the four sides of the semiconductor pellet 2.

[0044]

The second electrode pads 1A on the base substrate 1 are arranged in both side areas on the back surface of the base substrate 1 partitioned by the slits 5. Electric power, for example, an operating potential (e.g., 3.3 [V]) or a reference potential (e.g., 0 [V]), is applied to the second electrode pads 1A arranged in one area (an inner area with respect to the semiconductor pellet 2) of the back surface of the base substrate 1 partitioned by the slits 5. On the other hand, a

signal, e.g., an input/output signal or control signal, is applied to the second electrode pads 1A arranged in the other area (an outer area with respect to the semiconductor pellet 2) of the back surface of the base substrate 1 partitioned by the slits 5.

[0045]

In the semiconductor pellet 2, for example one hundred external terminals 2A are arranged for each side of the semiconductor pellet 2 and layout pitch thereof is set at, for example, 100 [μm] or so. The number of external terminals 2A is increased with an increase in the degree of integration and in the operating speed of the circuit system mounted on the semiconductor pellet 2.

[0046]

In the base substrate 1, the second electrode pads 1A arranged in one area of the back surface of the base substrate 1 partitioned by the slits 5 are arranged, for example, fifty for each side of the semiconductor pellet 2 and the second electrode pads 1A arranged in the other area of the back surface of the base substrate 1 partitioned by the slits 5 are arranged, for example, fifty for each side of the semiconductor pellet 2. Since the second electrode pads 1A cannot be microfabricated like the external terminals 2A of the semiconductor pellet 2, the layout pitch thereof is set wider than that of the external

terminals 2A and, for example, it is set at 200 [μm] or so. That is, the second electrode pads 1A of the base substrate 1 are arranged in two rows for each side of the semiconductor pellet 2, so even if the layout pitch of the second electrode pads 1A on the base substrate 1 is set twice as wide as that of the external terminals 2A on the semiconductor pellet 2, not only the layout length of the second electrode pads 1A for each side of the semiconductor pellet 2 can be made almost equal to that of the external terminals 2A arranged on one side of the semiconductor pellet 2, but also the second electrode pads 1A of the base substrate 1 can be arranged at positions opposed to the external terminals 2A of the semiconductor pellet 2.

[0047]

The peripheral area exclusive of the pellet mounting area of the main surface of the base substrate 1 is covered with a resinous sealing body 7 from above and the bonding wires 6 are sealed with the resinous sealing body 7. That is, the resinous sealing body 7 is formed on both main surface and back surface of the base substrate 1. For the purpose of attaining a lower stress, the resinous sealing body 7 is formed of an epoxy resin 7A incorporating a phenolic curing agent, silicone rubber and filler.

[0048]

A back surface opposite to the main surface of the

semiconductor pellet 2 is exposed from the resinous sealing body 7 which covers the peripheral area of the base substrate 1 from above.

[0049]

The resinous sealing body 7 is formed by a transfer molding method using a molding die 10 shown in Fig. 5 (a sectional view of a principal portion). The molding die 10 includes a cavity 11 formed by both an upper mold 10A and a lower mold 10B, an injection gate 13 connected to the cavity 11, as well as pot and runner (neither shown). The pot is connected to the cavity 11 through the runner and the injection gate 13.

[0050]

The cavity 11 is comprised of a recess 11A formed in the upper mold 10A and a recess 11B formed in the lower mold 10B. Resin (7A) is fed from the pot to the recess 11A through the runner and the injection gate 13. The base substrates 1 is loaded to the cavity 11B.

[0051]

Recesses 12 are formed in the recess 11B. The recesses 12 are arranged at positions opposed to the slits 5 of the base substrate 1 and are formed in the extending direction of the slits 5. A portion of the bonding wires for electrical connection between the external terminals (2A) of the semiconductor pellet 2 and the second electrode pads (1A) of

the base substrate 1 are arranged in each recess 12 and resin (7A) is fed from the recess 11A to the recesses 12 through the slits 5 of the base substrate 1.

[0052]

Though not shown, vent holes are formed in the recesses 12 for the purpose of preventing the formation of voids as a result of inclusion of bubbles.

[0053]

Next, a method for manufacturing the semiconductor device described above will be described below with reference to Figs. 6 to 9.

[0054]

First, a base substrate 1 comprised of a rigid substrate is provided. Slits 5 are formed in the base substrate 1 and second electrode pads (1A), first electrode pads (1B) and wiring lines ($1B_1$) are formed on a back surface side of the base substrate.

[0055]

Then, a semiconductor pellet 2 is mounted onto a pellet mounting area of the main surface of the base substrate 1. The semiconductor pellet 2 is fixed onto the pellet mounting area of the main surface of the base electrode 1 through an insulating layer 3.

[0056]

Next, the base substrate 1 is loaded onto a bonding state (heat block) 14 in a state in which the semiconductor pellet 2 faces down. A recess 14A for accommodating the semiconductor pellet 2 is formed in the bonding stage 14. The base substrate 1 and the semiconductor pellet 2 are heated to 200 [°C] or so at the bonding stage 14.

[0057]

Then, as shown in Fig. 7 (a sectional view of a principal portion), external terminals 2A arranged on a main surface of the semiconductor pellet 2 and second electrode pads (1A) arranged on the back surface of the base substrate 1 are connected together electrically using bonding wires 6. The bonding wires 6 are connected through the slits 5 of the base substrate 1 to the external terminals 2A of the semiconductor pellet 2 and also to the second electrode pads (1A) of the base substrate 1. Connection of the bonding wires 6 is performed by a bonding method which uses thermocompression bonding in combination with ultrasonic oscillation. In this process, since the base substrate 1 is a rigid substrate high in Young' modulus and hard as compared with a flexible substrate, a bonding load to be applied to the second electrode pads (1A) is not absorbed by the base substrate 1 and both bonding load and ultrasonic oscillation can be transmitted effectively to the second electrode pads (1A). Besides, since the base

substrate 1 is a rigid substrate which, as compared with a flexible substrate, is small in thermal expansion coefficient in a planar direction, high in Young's modulus and difficult to bend, it is possible to decrease a positional deviation of the second electrode pads (1A) and that of the external terminals 2A of the semiconductor pellet 2 both caused by a thermal expansion of the base substrate 1.

[0058]

Next, as sown in Fig. 8 (a sectional view of a principal portion), the base substrate 1 and the semiconductor pellet 2 are arranged within the cavity 11 formed by both upper and lower molds 10A, 10B of the molding die 10 and the base substrate 1 is loaded into the recess 11B of the cavity 11. A portion of the bonding wires 6 and the second electrode pads (1A) of the base substrate 1 are arranged within the recesses 12 formed in the recess 11B. The molding die 10 is heated beforehand to a temperature of about 170 to 180 [°C] in order to enhance the fluidity of the resin (7A) fed into the recess 11. In this process the base substrate 1 is heated to a temperature of about 170 to 180 [°C] as a result of heating of the molding die 10, but since the base substrate 1 is a rigid substrate small in thermal expansion coefficient in a planar direction, high in Young's modulus and difficult to bend as compared with a flexible substrate, it is possible to prevent deformation such

as warping or twisting of the base substrate 1 caused by heating of the molding die 10.

[0059]

Then, resin tablets are introduced into the pot of the molding die 10. The resin tablets are heated beforehand with a heater to lower the viscosity thereof and thereafter introduced into the pot. The resin tablets thus introduced into the pot are given heat from the molding die 10 and the viscosity thereof is further lowered thereby.

[0060]

Next, the resin tablets are pressurized by a plunger of a transfer molding apparatus and the resin 7A is fed from the pot into the recesses 11A and 12 of the cavity 11 through the runner and injection gate 13 to form a resinous sealing body 7 which, as shown in Fig. 9 (a sectional view of a principal portion), covers the peripheral area of the main surface of the base substrate 1, allows the back surface of the semiconductor pellet 2 to be exposed and seals the bonding wires 6. The resin 7A for the recesses 12 is fed through the slits 5 of the base substrate 1 from the recess 11A. In this process, since the resin 7A fed from the recess 11A to the recesses 12 through the slits 12 flows axially, namely, longitudinally of the bonding wires 6 from one end side of the wires, it is possible to prevent deformation of the bonding wires 6 caused by flowing of the resin

as compared with the case where the resin flows planarly, namely, laterally, of the base substrate 1.

[0061]

Then, the base substrate 1 is taken out from the molding die 10 and bump electrodes 4 are connected electrically and mechanically to the surfaces of the first electrode pads 1B formed on the back surface of the base substrate 1, whereby the semiconductor device shown in Figs. 1, 2, 3 and 4 is almost completed.

[0062]

Thereafter, the semiconductor device is shipped as product. As shown in Fig. 10 (a sectional view) thus shipped as product is mounted onto a mounting surface of a mounting substrate 15 and the bump electrodes 4 of the semiconductor device are connected electrically and mechanically to electrode pads 15A arranged on the mounting surface of the mounting substrate 15. The connection between the bump electrodes 4 of the semiconductor device and the electrode pads 15A of the mounting substrate 15 is performed in a reflow temperature atmosphere of about 210 to 230 [°C] though different depending on the material of the bump electrodes 4. In this mounting process it is possible to prevent deformation of the base substrate 1 caused by the reflow heat generated in the same process because the base substrate 1 is a rigid substrate small

in thermal expansion coefficient in a planar direction, high in Young's modulus and difficult to bent as compared with a flexible substrate.

[0063]

Thus, the following functions and effects are obtained according to this first embodiment.

[0064]

(1) In the semiconductor device wherein the semiconductor pellet 2 is mounted on the pellet mounting area of the main surface of the base substrate 1 and the first electrode pads 1B arranged on the back surface of the base substrate 1 are connected electrically to the external terminals 2A arranged on the main surface of the semiconductor pellet 2, the base substrate 1 is comprised of a rigid substrate, the first electrode pads 1B of the base substrate 1 are connected electrically to second electrode pads 1A arranged on the back surface of the base substrate 1, the semiconductor pellet 2 is mounted onto the pellet mounting area of the main surface of the base substrate 1 with its main surface facing down, and the external terminals 2A of the semiconductor pellet 2 and the second electrode pads 1A of the base substrate 1 are connected together electrically using bonding wires 6 through slits 5 formed in the base substrate 1. According to this construction, the external terminals 2A of the semiconductor pellet 2 and the

electrode pads 1B of the base substrate 1 can be connected together electrically through bonding wires 6 and electrode pads 1A, so that through-hole wiring lines for electrical connection between the second electrode pads 1A and the first electrode pads 1B can be omitted. As a result, the outline size of the base substrate 1 can be reduced to a degree corresponding to the area (land region area) occupied by the through-hole wiring lines and hence it is possible to attain the reduction in size of the semiconductor device.

[0065]

Since the first electrode pads 1B can be drawn closer to the second electrode pads 1A by a distance corresponding to the area occupied by the through-hole wiring lines, it is possible to shorten the wiring liens $1B_1$ of the base substrate 1 which lines provide electrical connections between the electrode pads 1A and 1B. As a result, it is possible to diminish inductance and hence possible to attain a high operating speed of the semiconductor device.

[0066]

The rigid substrate is high in Young's modulus and hard as compared with the flexible substrate, so when connecting the external terminals 2A arranged on the main surface of the semiconductor pellet and the second electrode pads 1A arranged on the back surface of the base substrate 1 electrically with

each other through bonding wires 6, a bonding load to be applied to the second electrode pads 1A is not absorbed by the base substrate 1 and both bonding load and ultrasonic oscillation are transmitted effectively to the second electrode pads 1A. As a result, it is possible to enhance the connection strength between the bonding wires 6 and the second electrode pads 1A and hence possible to prevent a connection defect of the bonding wires 6 and enhance the electrical reliability of the semiconductor device.

[0067]

The rigid substrate, as compared with the flexible substrate, is small in thermal expansion coefficient in a planar direction, high in Young's modulus and difficult to bend, so when mounting the semiconductor device onto the mounting surface of the mounting substrate 15, it is possible to prevent deformation (e.g., warping or twisting) of the base substrate 1 caused by reflow heat generated in the mounting process. As a result, it is possible to ensure the flatness of the back surface of the base substrate 1 with respect to the mounting surface of the mounting substrate 1 and hence possible to enhance the semiconductor device mounting accuracy.

[0068]

Since the rigid substrate is small in thermal expansion coefficient in a planar direction, high in Young's modulus and

difficult to bend as compared with the flexible substrate, it is possible to suppress warping of the base substrate 1 to 100 [μm] or less even if the outline size of the base substrate 1 increases with increase in the number of electrode pads 1B.

[0069]

Since warping of the base substrate 1 can be suppressed to 100 [μm] or less, it is possible to omit a reinforcing substrate which is provided for the purpose of preventing warp of the base substrate 1. As a result, it is possible to reduce the manufacturing cost of the semiconductor device as compared with a semiconductor device provided with such a reinforcing substrate.

[0070]

Since the base substrate 1 can be comprised of a printed wiring substrate of a single layer structure with second electrode pads 1A, first electrode pads 1B and wiring lines $1B_1$ arranged on the back surface of a rigid substrate, it is possible to reduce the parts cost of the base substrate 1 as compared with a base substrate comprised of a printed wiring substrate of two layers arranged on a main surface and a back surface of a rigid substrate. As a result, it is possible to reduce the semiconductor device manufacturing cost.

[0071]

(2) The slits are formed in the layout direction of the

external terminals 2A arranged plurally on the main surface of the semiconductor pellet 2 and are arranged over the external terminals 2A of the semiconductor pellet 2. According to this construction, since the slits 5 are arranged within the area occupied by the semiconductor pellet 2, it is possible to suppress an increase in outline size of the base substrate 1 corresponding to the area occupied by the slits 5.

[0072]

(3) The electrode pads 1A are arranged in both side areas of the back surface of the base substrate 1 partitioned by the slits 5. According to this construction it is possible to increase the power supply paths which provide electrical connections between the external terminals 2A of the semiconductor pellet 2 and the second electrode pads 1A of the base substrate 1. Consequently, it is possible to reduce power noise generated at the time of simultaneous switching of signals and hence possible to prevent a malfunction of the semiconductor device.

[0073]

Moreover, even if the layout pitch of the second electrode pads 1A of the base substrate 1 is set wider than that of the external terminals 2A of the semiconductor pellet 2, the pad layout length of the second electrode pads 1A for each side of the semiconductor pellet 2 can be made almost equal to that of the external terminals 2A arranged on each side of the

semiconductor pellet 2. Consequently, it is possible to prevent an increase in length of the bonding wires 6 attributable to the pad layout length of the second electrode pads 1A and, at the time of sealing the bonding wires 6 with the sealing body 7 in accordance with the transfer molding method, it is possible to prevent wire deformation of the bonding wires 6 caused by flowing of resin.

[0074]

Further, since the second electrode pads 1A of the base substrate 1 can be arranged at the position opposed to the external terminals 2A of the semiconductor pellet 2, the bonding wires 6 can be made uniform in length and hence it is possible to make uniform the inductance of the signal paths between the external terminals 2A of the semiconductor pellet 2 and the second electrode pads 1A of the base substrate 1.

[0075]

(4) The back surface opposed to the main surface of the semiconductor pellet 2 is exposed from the resinous sealing body 7 which covers the peripheral area of the main surface of the base substrate 1 from above. According to this construction, the heat generated with operation of the circuit system mounted on the semiconductor pellet 2 can be released to the exterior from the back surface of the semiconductor pellet 2, so that it is possible to enhance the heat dissipating efficiency of

the semiconductor device.

[0076]

Since the mechanical strength of the base substrate 1 can be compensated for by the mechanical strength of the resinous sealing body 7, it is possible to prevent deformation (e.g., warping or twisting) of the base substrate 1 caused by reflow heat in the mounting process.

[0077]

(5) The bonding wires 6 are sealed with the resinous sealing body 7. According to this construction, it is possible to prevent deformation of the bonding wires 6 caused by external shock or contact and hence possible to enhance the electrical reliability of the semiconductor device.

[0078]

(6) The resinous sealing body 7 is formed on both main surface and back surface of the base substrate 1. According to this construction, it is possible to prevent the resinous sealing body 7 from being peeled from the base substrate 1 due to a thermal stress generated in a temperature cycle test or at the time of connection of the bump electrodes 4 and hence possible to enhance the reliability of the semiconductor device.

[0079]

(7) In the semiconductor device manufacturing method wherein the semiconductor pellet 2 is mounted on the pellet mounting

area of the main surface of the base substrate 1 and the first electrode pads 1B arranged on the back surface of the base substrate 1 are connected electrically to the external terminals 2A arranged on the main surface of the semiconductor pellet 2, the method comprising the steps of mounting the semiconductor pellet 2 onto the pellet mounting area of the main surface of the base substrate 1 comprised of a rigid substrate in a state in which the main surface of the semiconductor pellet 2 faces down and connecting the external terminals 2A of the semiconductor pellet 2 and the second electrode pads 1A electrically with each other using bonding wires 6 through the slits 5 formed in the base substrate 1, the second electrode pads 1A being arranged on the back surface of the base substrate 1. Thus, since the external terminals 2A of the semiconductor pellet 2 and the first electrode pads 1B of the base substrate 1 are connected with each other electrically through the bonding wires 6 and the second electrode pads 1A, through-hole wiring lines (1C) for electrical connection between the second electrode pads 1A and the first electrode pads 1B are omitted and the base substrate 1 is reduced in outline size to a degree corresponding to the area occupied by the through-hole wiring lines. As a result, it is possible to manufacture a semiconductor device of a small outline size.

[0080]

Since the external terminals 2A of the semiconductor pellet 2 and the first electrode pads 1B of the base substrate 1 are connected electrically with each other through the bonding wires 6 and the second electrode pads 1A, through-hole wiring lines (1C) for electrical connection between the second electrode pads 1A and the first electrode pads 1B are omitted and the wiring lines $1B_1$ used in the base substrate 1 for electrical connection between the second electrode pads 1A and the first electrode pads 1B can be shortened to a degree corresponding to the area occupied by the through-hole wiring lines. As a result, it is possible to manufacture a semiconductor device high in operating speed.

[0081]

The base substrate 1 used is a rigid substrate which is high in Young's modulus and hard as compared with a flexible substrate, so when connecting the external terminals 2A arranged on the main surface of the semiconductor pellet 2 and the second electrode pads 1A arranged on the backs surface of the base substrate 1 electrically with each other through the bonding wires 6, a bonding load to be applied to the second electrode pad 1A is not absorbed by the base substrate 1 and both bonding load and ultrasonic oscillation are transmitted effectively to the second electrode pads 1A. As a result, it is possible to enhance the connection strength between the

bonding wires 6 and the second electrode pads 1A and hence possible to manufacture a semiconductor device high in electrical reliability.

[0082]

The base substrate 1 used is a rigid substrate small in thermal expansion coefficient in a planar direction, high in Young's modulus and difficult to bend as compared with a flexible substrate, so when mounting the semiconductor device onto the mounting surface of the mounting substrate 15, it is possible to prevent deformation (e.g., warping or twisting) of the base substrate 1 caused by reflow heat generated in the mounting process. As a result, it is possible to ensure flatness of the back surface of the base substrate 1 with respect to the mounting surface of the mounting substrate 15 and hence possible to manufacture a semiconductor device high in mounting accuracy.

[0083]

(8) The electrical connecting step using the bonding wires 6 is followed by the step of forming the resinous sealing body 7 by the transfer molding method, the resinous sealing body covering the peripheral area of the main surface of the base substrate 1 and sealing the bonding wires 6. In this case, since the base substrate 1 used is a rigid substrate small in thermal expansion coefficient in a planar direction, high in Young's

modulus and difficult to bent as compared with a flexible substrate, it is possible to prevent deformation such as warping or twisting of the base substrate 1 caused by heating of the molding die 10.

[0084]

Moreover, since the resin 7A fed from the recess 11A to the recesses 12 through the slits 5 flows axially, namely, longitudinally of the bonding wires 6 from one end side of the same wires, it is possible to prevent deformation of the bonding wires 6 caused by flowing the resin 7A in comparison with the case where the resin flows in a planar direction, namely, laterally of the base substrate 1.

[0085]

As shown in Fig. 11 (a sectional view), the resinous sealing body 7 may be formed on the back surface of the base substrate 1 exclusive of the surfaces of the second electrode pads 1A and the first electrode pads 1B. According to this shape the bases substrate 1 is sandwiched by the resinous sealing body 7 and therefore it is possible to prevent warping of the base substrate 1.

[0086]

Though not shown, the base substrate 1 may be of a laminate structure comprising plural rigid substrates stacked one on another. In this case, it is possible to reduce the

semiconductor manufacturing cost in comparison with a base substrate of a laminate structure comprising plural flexible substrates stacked one on another.

[0087]

(Second Embodiment)

A schematic construction of a semiconductor device adopting a BGA structure according to a second embodiment of the present invention is shown in Fig. 12 (a sectional view) and Fig. 13 (an enlarged plan view of a principal portion on a back surface side with a resinous sealing body on the back surface side removed).

[0088]

In the semiconductor device of this second embodiment, as shown in Figs. 12 and 13, a semiconductor pellet 2 is arranged on a pellet mounting area of a main surface of a base substrate 1 through an insulating layer 3 by a face-down method and plural bump electrodes 4 are arranged lattice-like on a back surface side of the base substrate 1.

[0089]

Plural external terminals 2A are arranged at a center of a main surface of the semiconductor pellet 2 and along long sides of the main surface. The external terminals 2A are connected respectively to plural second electrode pads 1A electrically using bonding wires 6 through a slit 5 formed in the base

substrate 1, the second electrode pads 1A being formed on the back surface of the base substrate 1. The second electrode pads 1A are connected respectively to plural first electrode pads 1B electrically through wiring lines $1B_1$, the electrode pads 1B being formed on the back surface of the base substrate 1. The bump electrodes 4 are connected respectively onto the surfaces of the first electrode pads 1B electrically and mechanically. That is, the external terminals 2A of the semiconductor pellet 2 are connected to the first electrode pads 1B electrically through bonding wires 6, second electrode pads 1A and wiring lines $1B_1$.

[0090]

The slit 5 of the base substrate 1 is formed in the layout direction of the external terminals 2A which are arranged at a center of the main surface of the semiconductor pellet 2 and along long sides of the main surface. The slit 5 is formed in a tapered shape having an aperture size on the main surface side of the base substrate 1 smaller than that on the back surface side of the base substrate.

[0091]

Thus, according to this second embodiment, not only the same functions and effects as in the previous first embodiment are obtained, but also, by forming the slit 5 in a tapered shape, it is possible to prevent contact between the base substrate

1 and a bonding tool when bonding one ends of the bonding wires 6 to the external terminals 2A on the semiconductor pellet 2, so that it is possible to enhance the semiconductor device assembling yield in the bonding process.

[0092]

(Third Embodiment)

A schematic construction of a semiconductor device adopting a BGA structure according to a third embodiment of the present invention is shown in Fig. 14 (a plan view of a principal portion on a back surface side with a resinous sealing body on the back surface side removed).

[0093]

In the semiconductor device of this third embodiment, as shown in Fig. 14, a semiconductor pellet 2 is mounted onto a pellet mounting area of a main surface of a base substrate 1 through an insulating layer (3) by a face-down method and plural bump electrodes 4 are arranged lattice-like on a back surface side of the base substrate 1.

[0094]

Plural external terminals 2A are arranged on the outer periphery of a main surface of the semiconductor pellet 2 and along four sides of the main surface. Further, at the center of the main surface of the semiconductor pellet 2 there are arranged plural external terminals 2A along long or short sides

of the main surface. The external terminals 2A are coupled respectively to plural second electrode pads 1A electrically using bonding wires 6 through slits 5 formed in the base substrate 1, the second electrode pads 1A being arranged on the back surface of the base substrate 1. The second electrode pads 1A are connected respectively to plural first electrode pads 1B electrically through wiring lines ($1B_1$), the first electrode pads 1B being arranged on the back surface of the base substrate 1. Bump electrodes 4 are connected respectively onto the surfaces of the first electrode pads 1B electrically and mechanically. That is, the external terminals 2A of the semiconductor pellet 2 are connected to the first electrode pads 1B electrically through bonding wires 6, second electrode pads 1A and wiring lines $1B_1$.

[0095]

The slits 5 of the base substrate 1 are positioned not only on each side but also at the center of the semiconductor pellet 2. That is, in this third embodiment, five slits 5 are formed in the base substrate 1. The five slits 5 are arranged over the external terminals 2A of the semiconductor pellet 2.

[0095]

Thus, according to this third embodiment there are obtained the same functions and effects as in the foregoing first embodiment. Besides, by arranging the slits 5 on each

side of the semiconductor pellet 2 and also at the center of the semiconductor pellet, not only it is possible to increase the number of external terminals 2A arranged on the main surface of the semiconductor pellet 2 but also increase the number of second electrode pads 1A arranged on the back surface of the base substrate 1, so that it is possible to increase the power supply paths which provide electrical connections between the external terminals 2A of the semiconductor pellet 2 and the electrode pads 1A of the base substrate 1. Consequently, it is possible to further reduce power noise generated at the time of simultaneous switching of output signals. Moreover, it is possible to increase the signal paths which provide electrical connections between the external terminals 2A of the semiconductor pellet 2 and the second electrode pads 1A of the base substrate 1 and hence possible to reduce the outline size of the semiconductor pellet 2 which is restricted by the number of external terminals 2A.

[0097]

Although according to the construction of this third embodiment there is arranged one slit 5 at the center of the semiconductor pellet 2, plural slits 5 may be formed at the center of the semiconductor pellet 2 so as to be parallel or intersect each other, thus increasing the number of slits 5, whereby the number of second electrode pads 1A of the base

substrate 1 and that of the external terminals 2A of the semiconductor pellet 2 can be further increased.

[0098]

(Fourth Embodiment)

A schematic construction of a semiconductor device adopting a BGA structure according to a fourth embodiment of the present invention is shown in Fig. 15 (a plan view of a principal portion on a back surface side with a resinous sealing body on the back surface side removed).

[0099]

In the semiconductor device of this fourth embodiment, as shown in Fig. 15, a semiconductor pellet 2 is mounted onto a pellet mounting area of a main surface of a base substrate 1 through an insulating layer (3) by a face-down method and plural bump electrodes 4 are arranged lattice-like on a back surface side of the base substrate 1. For example, the base substrate 1 is a printed wiring substrate of a three-layer wiring structure.

[0100]

On the outer periphery of a main surface of the semiconductor pellet 2 there are arranged plural external terminals 2A along each side of the main surface. The external terminals 2A are connected respectively to plural second electrode pads 1A electrically using bonding wires 6 through

slits formed in the base substrate 1, the second electrode pads 1A being arranged on the back surface of the base substrate 1.

[0101]

Of the second electrode pads 1A, electrode pads $1A_2$ are formed integrally with electrode plates 8A. One electrode plate 8A is connected electrically to another electrode plate 8A through a through-hole wiring line (not shown) and an internal wiring line (not shown) of the base substrate 1. A reference potential (e.g., 0 [V]) is applied as electric power to each electrode plate 8A. Of the second electrode pads 1A, electrode pads $1A_3$ are formed integrally with an electrode plate 8B. For example, an operating potential (e.g., 3.3 [V]) is applied as electric power to the electrode plate 8A.

[0102]

Thus, according to this fourth embodiment, through-hole wiring lines (1C) for electrical connection between the second electrode pads (1A) arranged on the main surface of the base substrate 1 and the first electrode pads 1B arranged on the back surface of the base substrate are omitted, whereby the electrode plates 8A and 8B can be arranged on the back surface side of the base substrate 1. Consequently, the layout of the bump electrodes 4 can be set freely and it is possible to shorten the distance between the external terminals 2A of the semiconductor pellet 2 and the bump electrodes 4. As a result,

it is possible to decrease inductance and hence possible to attain a high operating speed of the semiconductor device.

[0103]

Although the present invention has been described above concretely by way of the above embodiments, it goes without saying that the invention is not limited to the above embodiments, but that various changes may be made within the scope not departing from the gist of the invention.

[0104]

[Effect of the Invention]

The following is a brief description of effects obtained by typical modes of the present invention as disclosed herein.

[0105]

It is possible to reduce the size of a semiconductor device wherein a semiconductor pellet is mounted on a pellet mounting surface of a main surface of a base substrate and first electrode pads arranged on a back surface of the base substrate are connected electrically to external terminals arranged on a main surface of the semiconductor pellet.

[0106]

Moreover, it is possible to attain a high operating speed of the semiconductor device.

[0107]

Further, it is possible to enhance the electrical

reliability of the semiconductor device.

[0108]

Additionally, it is possible to enhance the mounting accuracy of the semiconductor device.

[Brief Description of the Drawings]

Fig. 1 is a plan view of a main surface side of a semiconductor device adopting a BGA structure according to a first embodiment of the present invention.

Fig. 2 is a sectional view taken on line A-A in Fig. 1.

Fig. 3 is an enlarged sectional view of a principal portion in Fig. 2.

Fig. 4 is an enlarged plan view of a principal portion on a back surface side of the semiconductor device with a resinous sealing body on the back surface side removed.

Fig. 5 is a sectional view of a principal portion of a molding die for forming the resinous sealing body in the semiconductor device.

Fig. 6 is a sectional view to explain a method for manufacturing the semiconductor device.

Fig. 7 is a sectional view of a principal portion for explaining the semiconductor device manufacturing method.

Fig. 8 is a sectional view of a principal portion for explaining the semiconductor device manufacturing method.

Fig. 9 is a sectional view of a principal portion for

explaining the semiconductor device manufacturing method.

Fig. 10 is a sectional view of a principal portion, showing a mounted state of the semiconductor device onto a mounting substrate.

Fig. 11 is a sectional view showing a modification of the semiconductor device.

Fig. 12 is a sectional view of a semiconductor device adopting a BGA structure according to a second embodiment of the present invention.

Fig. 13 is an enlarged plan view of a back surface side of the semiconductor device with a resinous sealing body on the back surface side removed.

Fig. 14 is a plan view of a principal portion of a back surface side of a semiconductor device adopting a BGA structure according to a third embodiment of the present invention, with a resinous sealing body on the back surface side removed.

Fig. 15 is a plan view of a principal portion of a back surface side of a semiconductor device adopting a BGA structure according to a fourth embodiment of the present invention, with a resinous sealing body on the back surface side removed.

Fig. 16 is a sectional view of a principal portion of a conventional semiconductor device adopting a BGA structure.

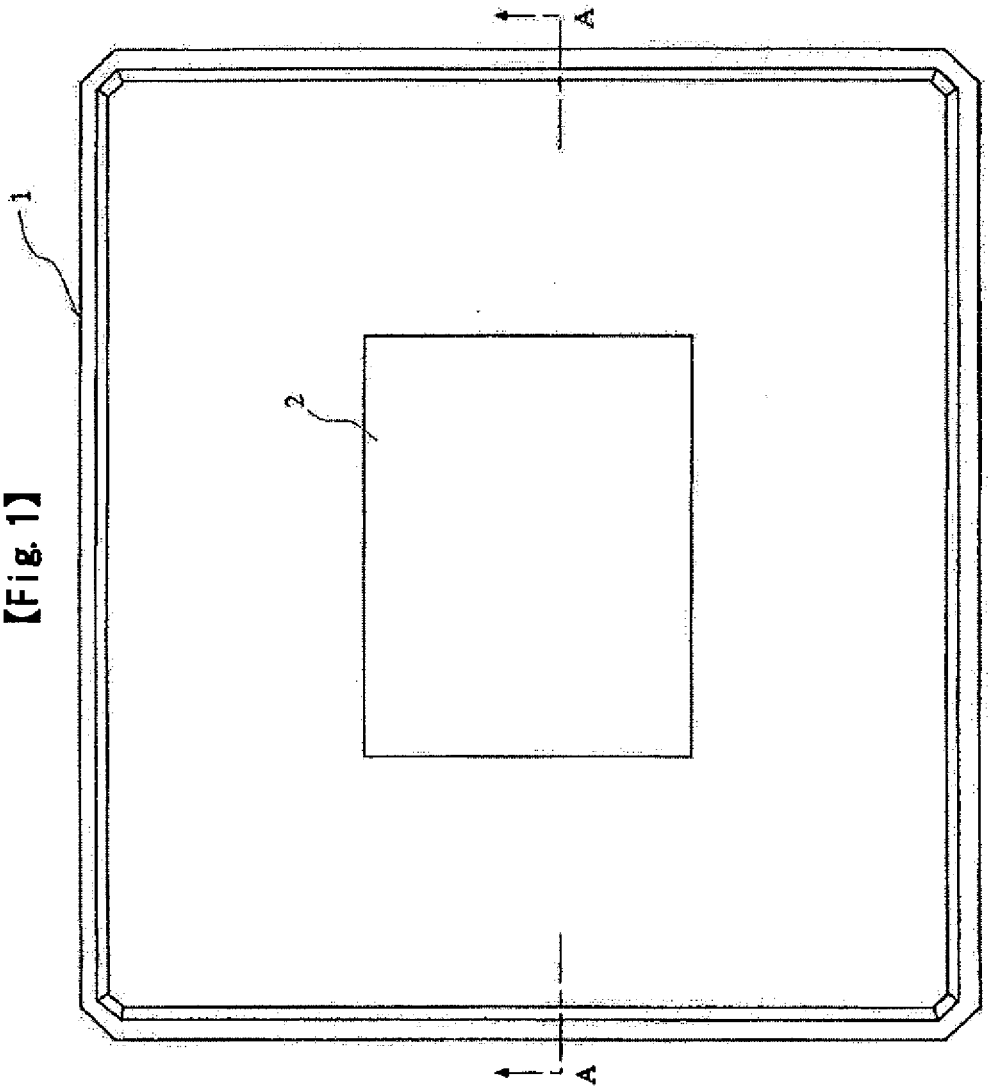
[Explanation of Reference Numerals]

1 ... base substrate, 1A ... electrode pad, 1B ... electrode

pad, 2 ... semiconductor pellet, 2A ... external terminal, 3 ... insulating layer, 4 ... bump electrode, 5 ... slit, 6 ... bonding wire, 7 ... resinous sealing body, 7A... resin, 8A, 8B ... electrode plate, 10 ... molding die, 10A ... upper mold, 10B ... lower mold, 11 ... cavity, 11A, 11B, 12 ... recess, 13 ... injection gate, 14 ... heat stage, 14A ... recess, 15 ... mounting substrate, 15A ... electrode pad

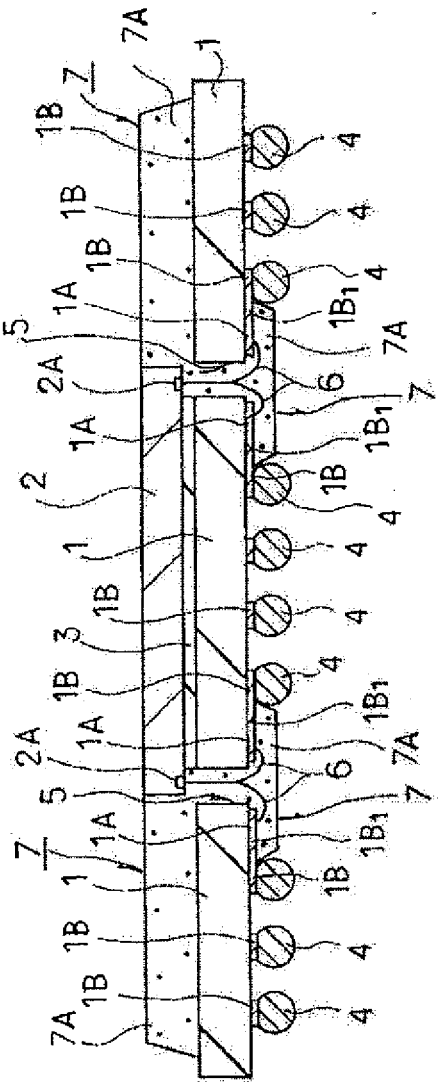
【Name of Document】 Drawing

【Fig.1】



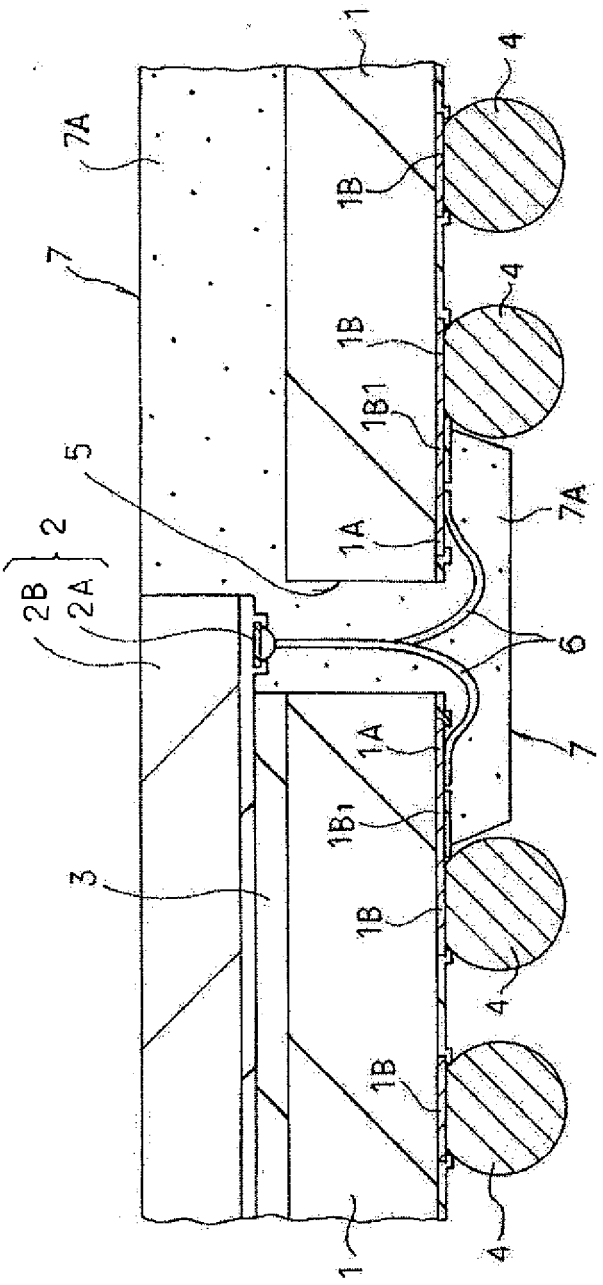
【Fig. 1】

【Fig.2】

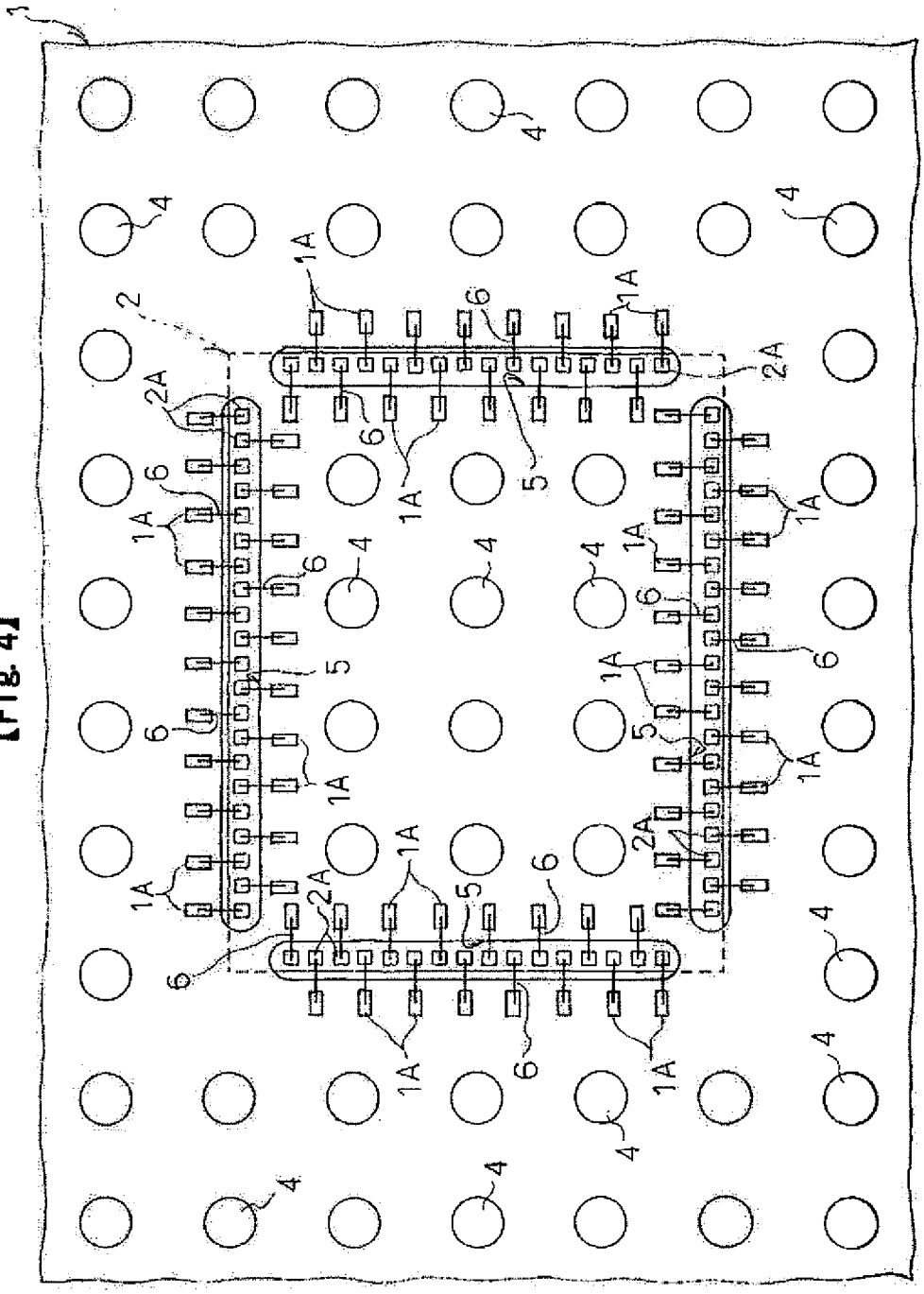


【Fig.3】

【Fig. 3】

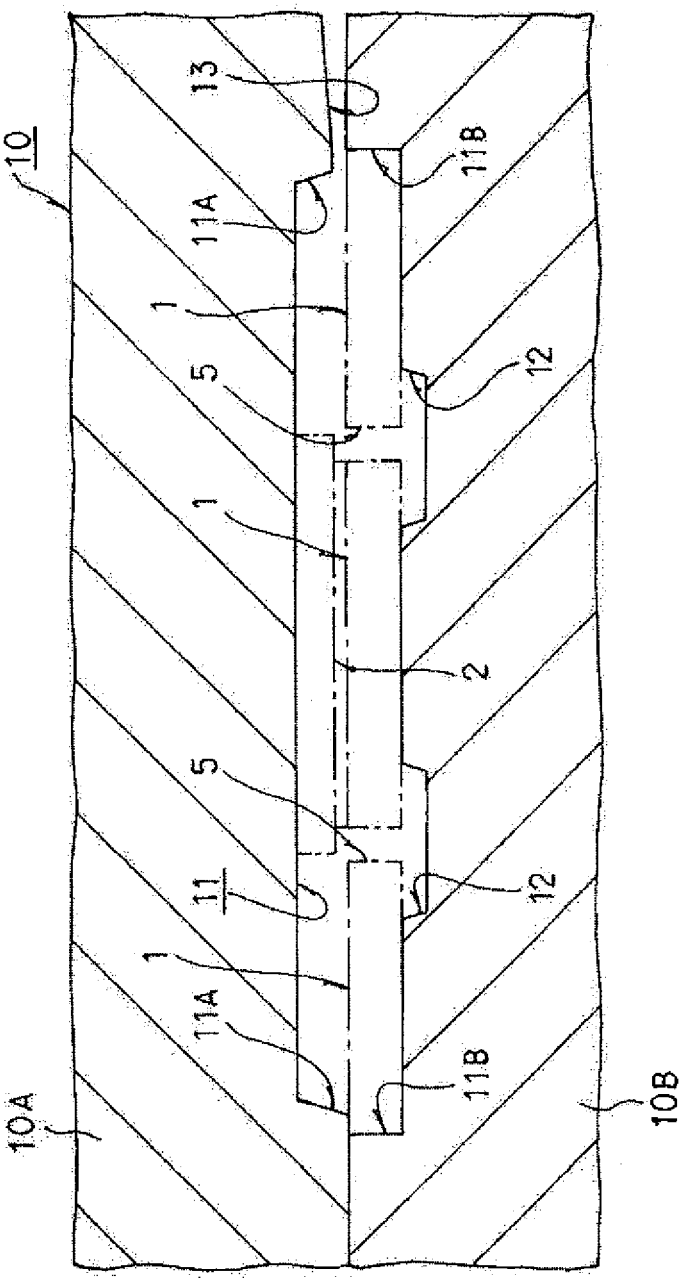


【Fig.4】



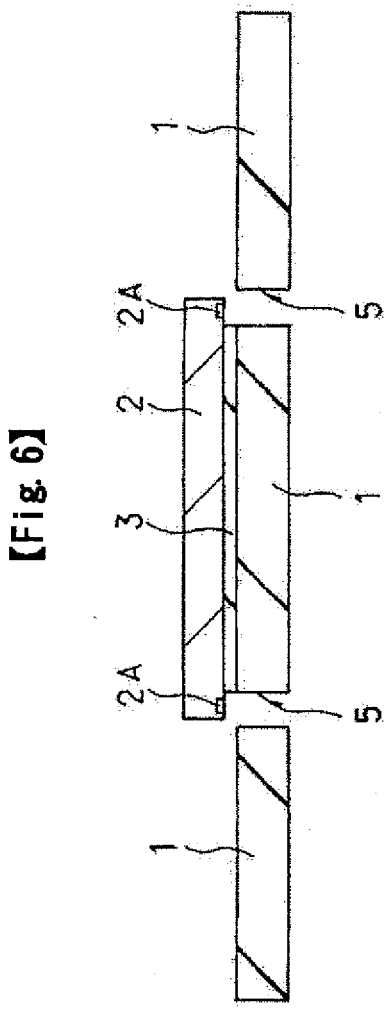
【Fig. 4】

【Fig.5】



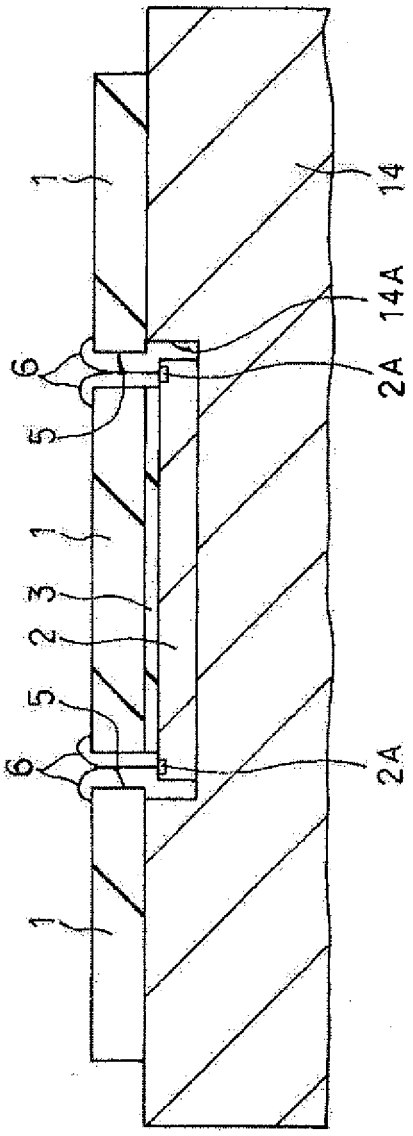
【Fig. 5】

【Fig.6】



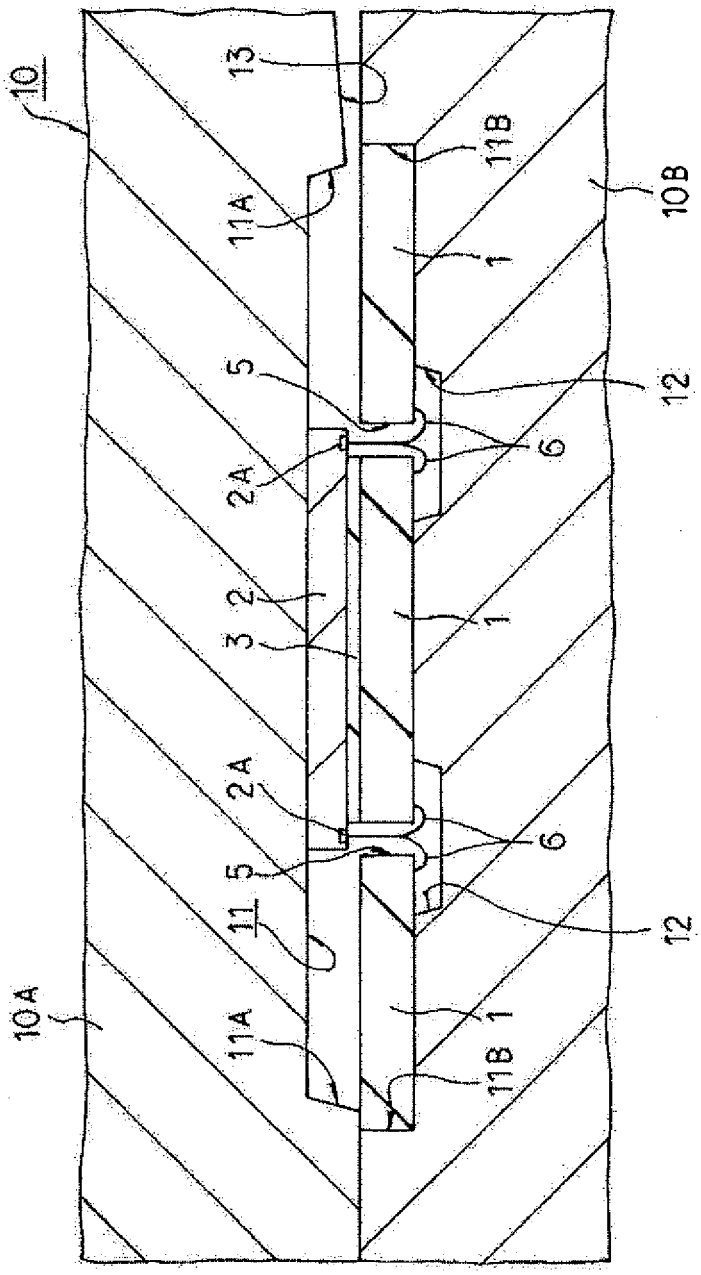
【Fig. 6】

【Fig.7】



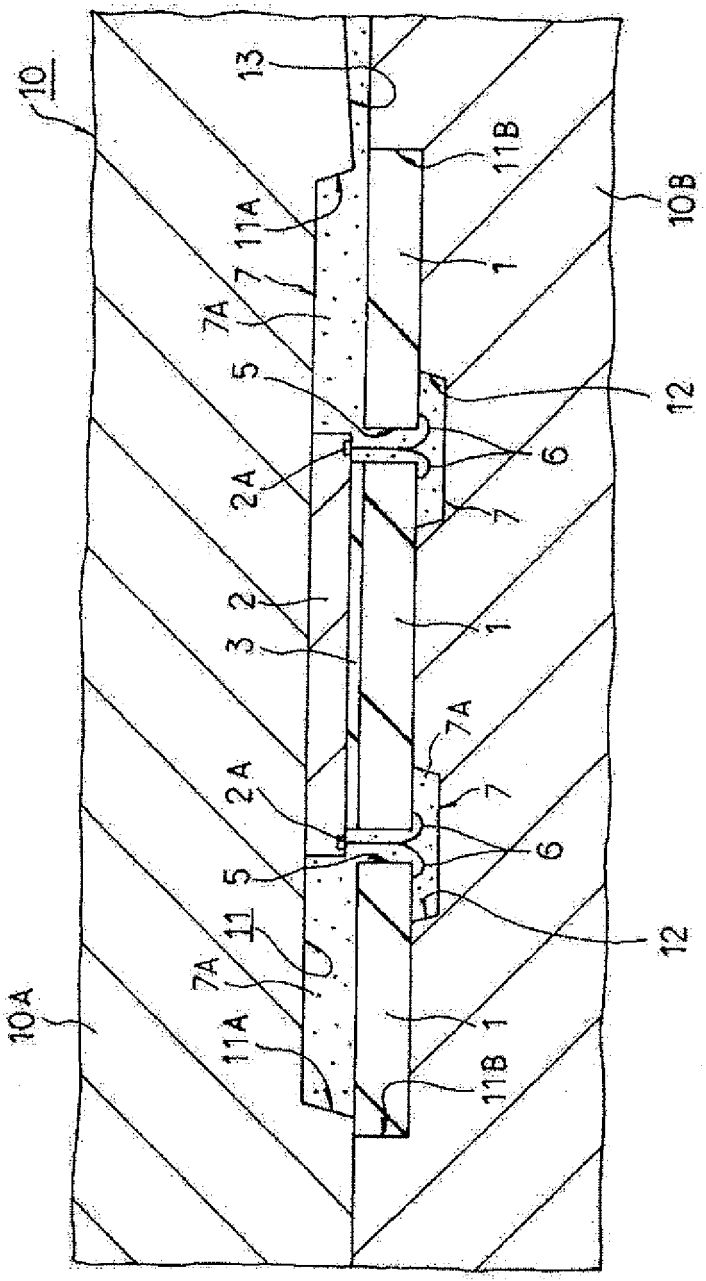
【Fig. 7】

【Fig.8】



【Fig. 8】

【Fig.9】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10B
11A
7
7A
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5
12
6
2A
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2
3
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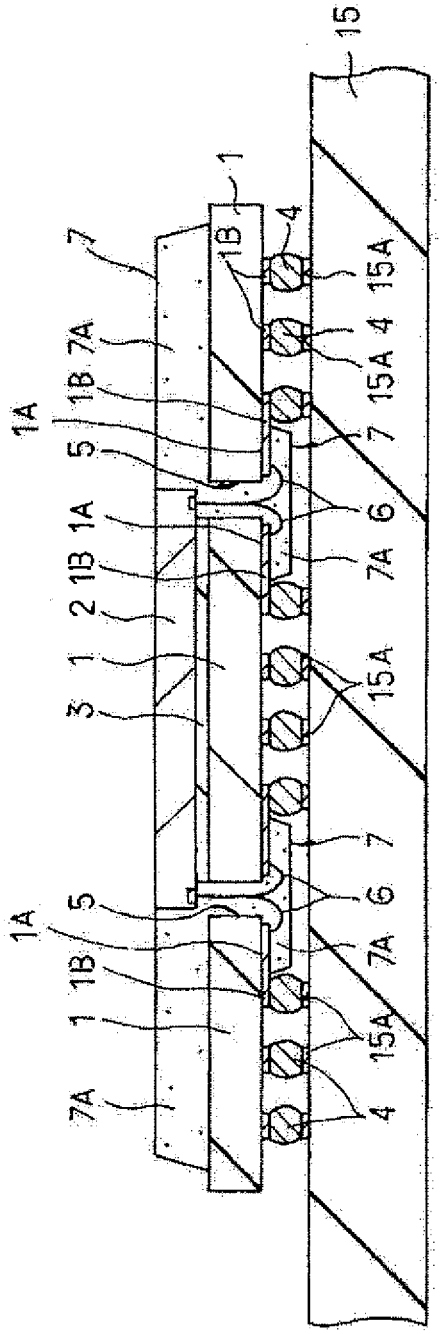
11
12
7A
10A
11A
11B
1

【Fig. 9】

【Fig.10】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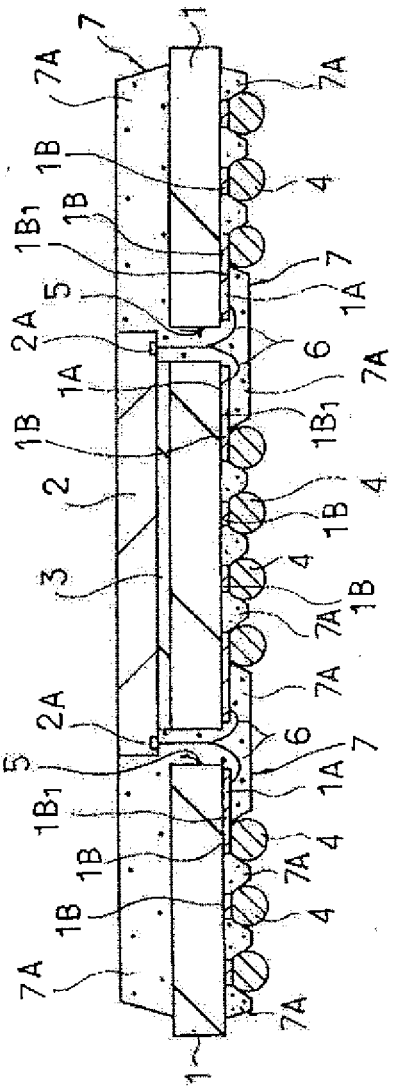
1B
4
7
7A
1B
1A
5
1A
1B
2
1
3
1A
5
1B
7A
4
15A
1
15A
4
15A
7
6
7A
15A
7
6
7A
15A
4

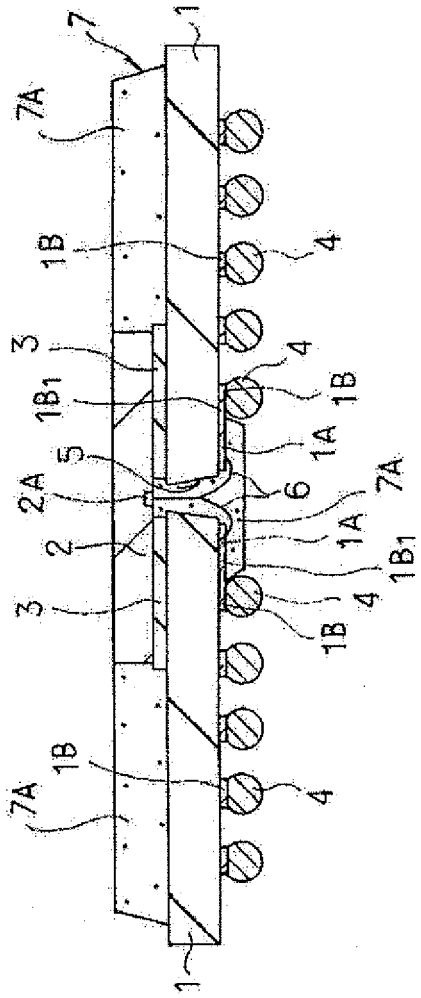
【Fig. 10】

【Fig.11】



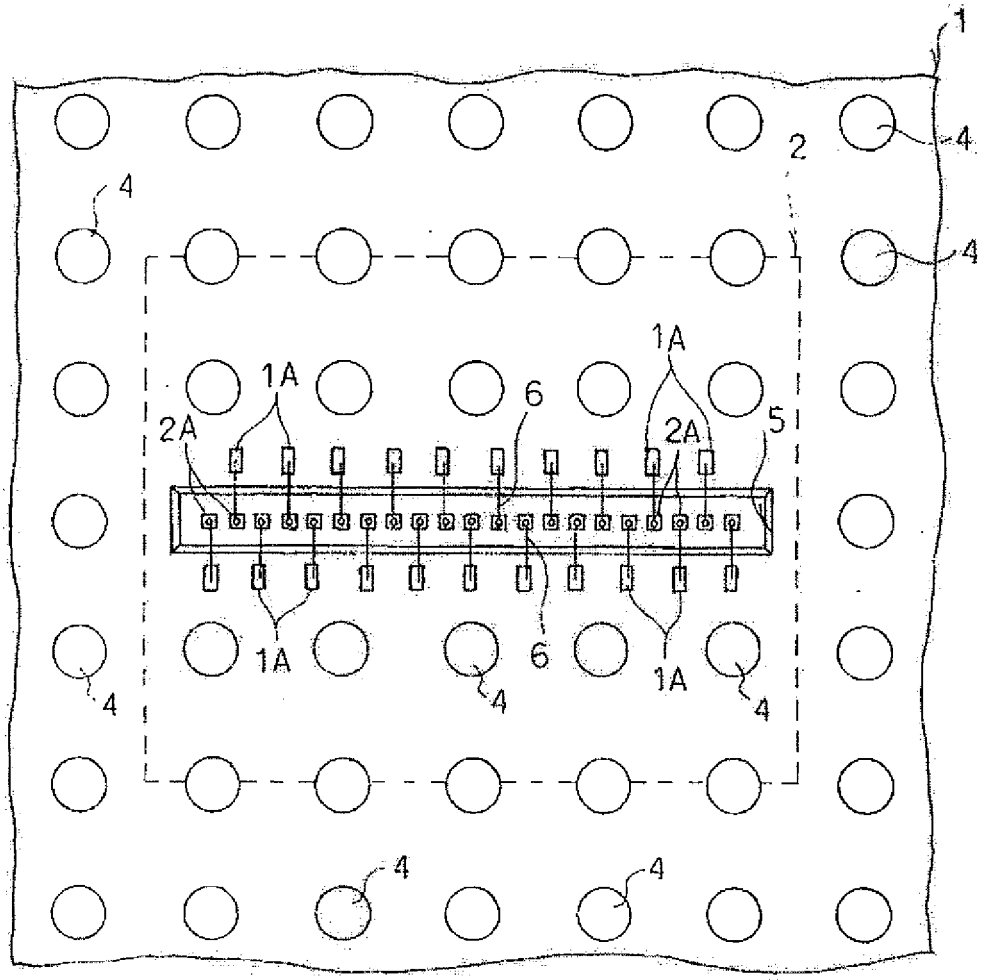
【Fig.12】

【Fig. 12】

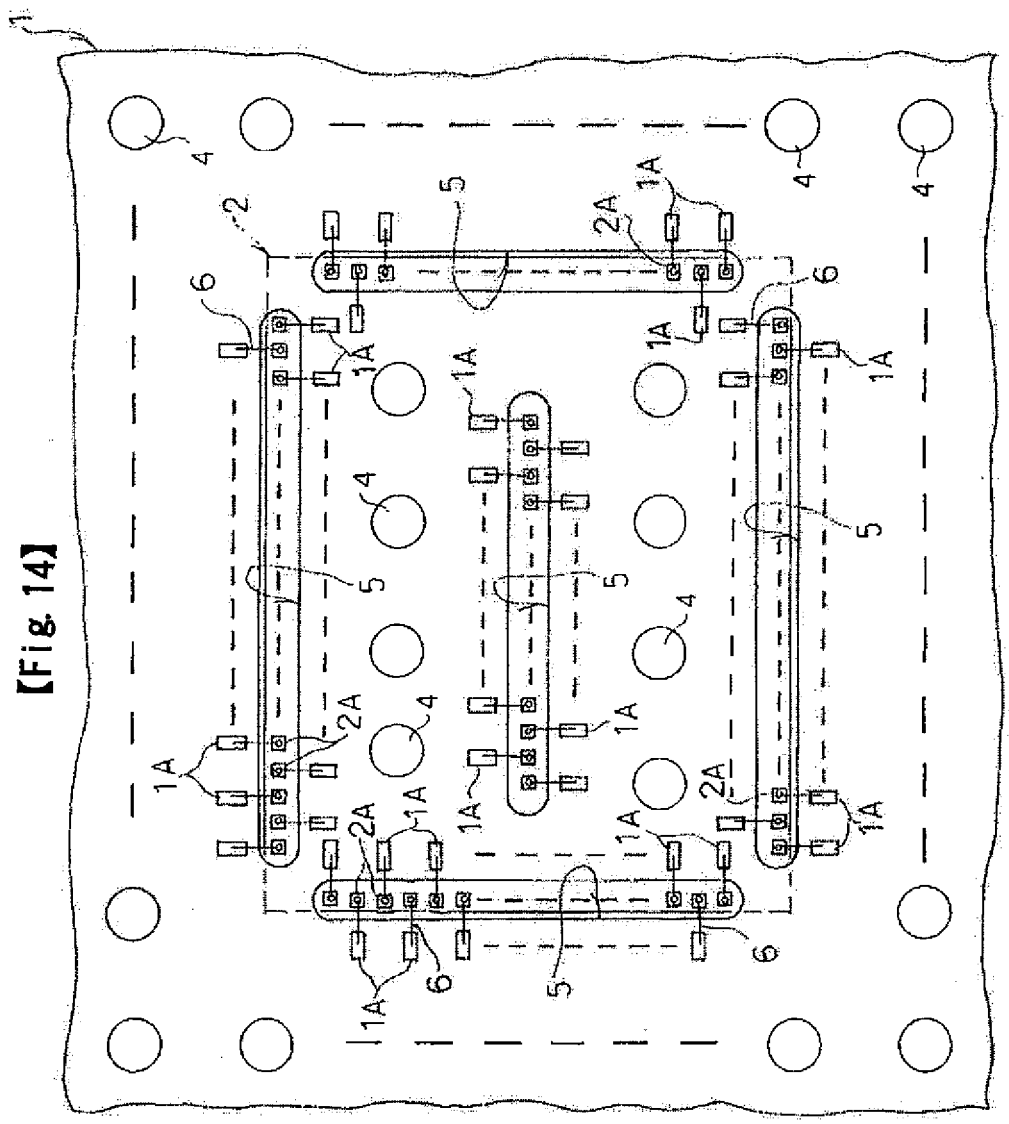


【Fig.13】

【Fig. 13】



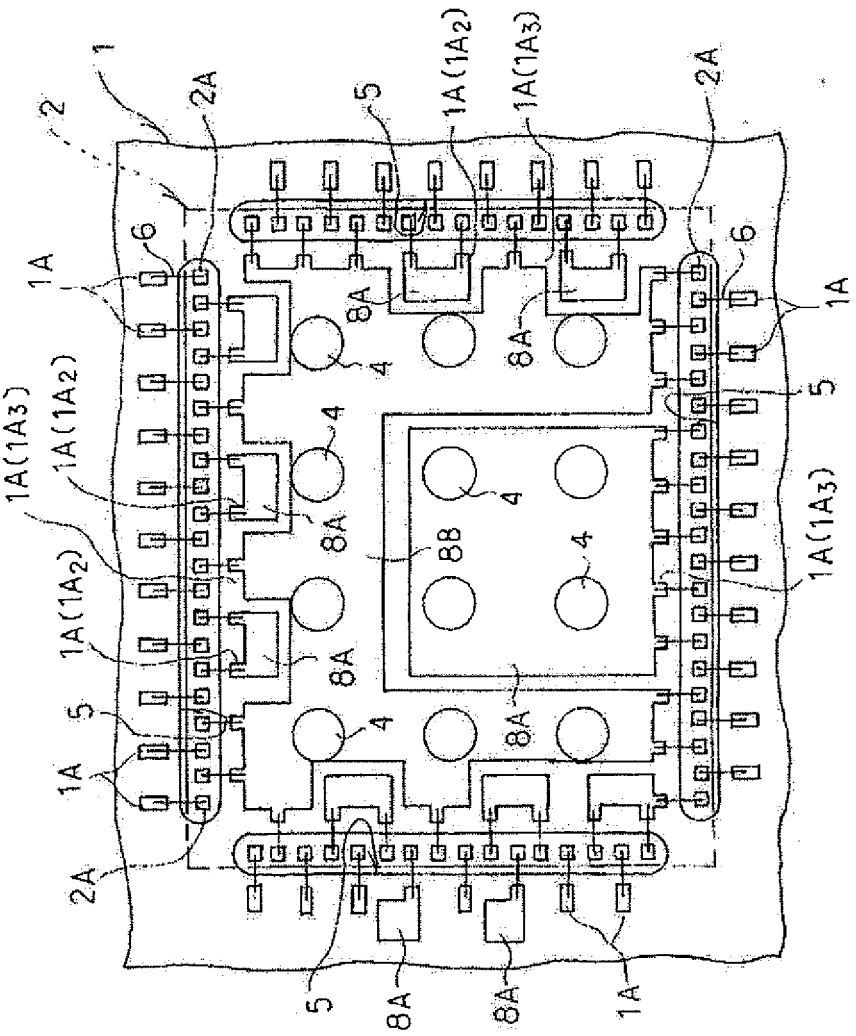
【Fig.14】



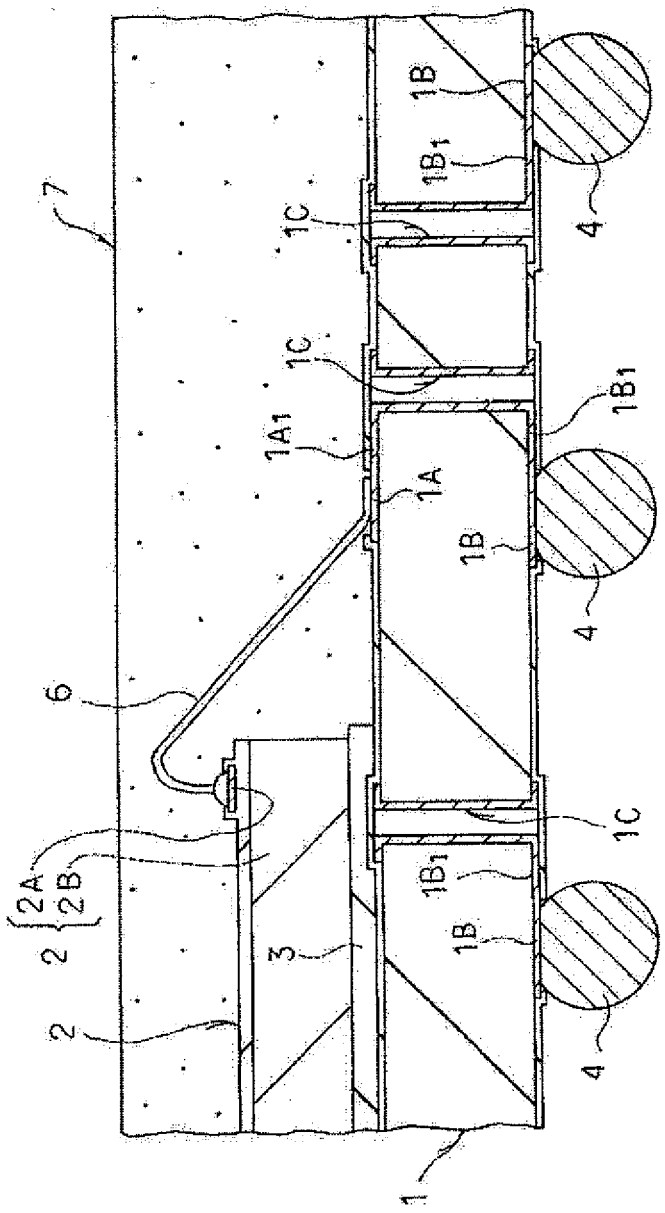
【Fig. 14】

[Fig.15]

【Fig. 15】



【Fig.16】



【Fig. 16】

[Name of Document] Abstract

[Abstract]

[Object]

The size of a semiconductor device is to be reduced, a high operating speed of the semiconductor device is to be attained, and mounting accuracy is enhanced.

[Construction]

A semiconductor device comprising a base substrate 1, a semiconductor pellet 2 mounted on a pellet mounting area of a main surface of the base substrate 1, external terminals 2A arranged over a main surface of the semiconductor pellet 2, and first electrode pads 1B arranged over a back surface of the base substrate 1 and coupled electrically to the external terminals 2A, the semiconductor pellet 2 being mounted on the pellet mounting area of the main surface of the base substrate 1 in a state in which the main surface of the semiconductor pellet 2 faces down, second electrode pads coupled electrically to the first electrode pads being arranged over the back surface of the base substrate 1, and the external terminals 2A of the semiconductor pellet 2 and the second electrode pads 1A of the base substrate 1 being coupled together electrically with bonding wires 6 through a slit 5 formed in the base substrate 1.

[Selected Drawing] Fig. 3